Please enter the following as a complete listing of the claims in the present application:

1 – 21 (Canceled)

22. (Withdrawn) A chip scale package for a semiconductor device containing a plurality of electronic circuits, said chip scale package comprising:

a semiconductor body having a size and shape configured to accommodate the plurality of electronic circuits in the semiconductor device;

a via having a via top portion beginning at a top surface of said body and extending through said die to a via bottom portion on a bottom surface of said body;

an input/output (I/O) interconnect physically and electrically coupled to said via bottom portion, said I/O interconnect structure being located within an area on the bottom surface of said die; and

an I/O signal line formed of a conductive material passing through said via and coupled to said said I/O interconnect structure;

wherein said packaging for the device is formed prior to the formation of any of the plurality of electronic circuits.

23. (Withdrawn) The package of claim 22, further including a plurality of additional I/O interconnects, and wherein all of said I/O interconnects are located within a surface area corresponding to the bottom surface of said body.

24. (Withdrawn) The package of claim 22 wherein said electronic circuit and said I/O interconnects can be formed on opposite sides of said semiconductor body.

25. (Withdrawn) The package of claim 22, wherein said package is contained within a single semiconductor wafer including a plurality of additional identical packages.

26. (Withdrawn) The package of claim 22, wherein said vias are filled with a conductive material.

27. (Withdrawn) The package of claim 22, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said body.

28. (Withdrawn) The package of claim 22, wherein said I/O interconnect is a bottom side conductive pad located on the bottom side of said body.

29. (Withdrawn) The package of claim 28, wherein said top portion of said via is coupled to a top side conductive pad located on the top side of said die, and wherein said top side conductive pad is smaller than said bottom side conductive pad.

30. (Withdrawn) The package of claim 22, wherein said I/O interconnect includes a conductive bump structure.

31 – 48 **(Canceled)**

49. (Previously presented) A semiconductor wafer including an integrated chip scale package to be used for integrated circuits, the wafer comprising:

a top surface and a bottom surface; and

wherein the semiconductor wafer is an unprocessed wafer having no active circuit layers or interconnect layers present on said top surface or said bottom surface of the semiconductor wafer;

a plurality of vias formed in the unprocessed semiconductor wafer, each via having a via top portion beginning at said top surface of the unprocessed semiconductor wafer and extending through to a via bottom portion on said bottom surface of the unprocessed semiconductor wafer;

wherein at least some of said plurality of vias include an input/output (I/O) interconnect structure physically and electrically coupled to said via bottom portion, and said I/O interconnect structure is located within an area on the bottom surface of the unprocessed wafer; and

wherein the I/O interconnect structure is adapted such that an active circuit which is fabricated on the unprocessed semiconductor wafer as part of an integrated circuit at a later time than the I/O interconnect structure can be electrically connected to another integrated circuit without requiring further packaging operations to form pads or bumps for connecting I/O signals of such active circuit to such another integrated circuit.

50. (Previously presented) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with a conductive material capable of withstanding a high temperature cycle associated with a manufacturing operation used later to make said active circuit.

51. (Previously presented) The semiconductor wafer of claim 49, wherein at least some of said plurality of vias are filled with an insulating material capable of providing support for the semiconductor wafer during a manufacturing operation used later to make said active circuit.

52. (Previously presented) The semiconductor wafer of claim 49 wherein said via is substantially larger than a minimum feature size used in fabricating said active circuit.

53. (Previously presented) The semiconductor wafer of claim 52, wherein said via is about 4 mils in diameter.

54. (Previously presented) The semiconductor wafer of claim 49, further including a passivation layer formed on at least said top surface.

55. (Previously presented) The semiconductor wafer of claim 49, wherein the input/output (I/O) interconnect structure includes a plurality of solder bumps and/or pads.

56. (Previously presented) The semiconductor wafer of claim 49, wherein the semiconductor wafer includes a plurality of chip-scale packages.

57. (Previously presented) The semiconductor wafer of claim 55, further including a plurality of integrated circuits on the semiconductor wafer coupled to said plurality of chip-scale packages.

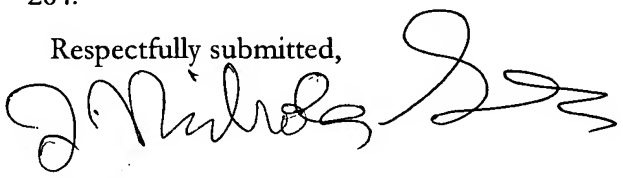
58. (Previously presented) The semiconductor wafer of claim 55, wherein said plurality of integrated circuits on the semiconductor wafer are memory devices.

59. (Previously presented) The semiconductor wafer of claim 55, further including a second I/O structure on a top surface of the semiconductor wafer.

60. (Previously presented) The semiconductor wafer of claim 55, wherein said bottom portion for at least some of said plurality of vias is substantially larger than a corresponding top portion.

No fees are believed to be due since the supplemental response was adequate within the requirements of the restriction requirement made by the Examiner. If any fees are due, please charge any fees to deposit account no. 233 - 264.

Respectfully submitted,



J. Nicholas Gross
Registration No. 34,175
Attorney for Applicants

March 30, 2005
726 Duboce Avenue
San Francisco, CA 94117
(415) 355 – 9800

I hereby certify that the foregoing is being deposited with the U.S. Postal Service to Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, this 30th day of March 2005.